

# An 83dB Low-Power High-Linearity Variable Gain Amplifier

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**Abstract**—A newly proposed variable gain amplifier (VGA) topology is presented. The three-stage VGA offers a wide control gain range, which is independent on process variation, and is characterized by low-power, high linearity, wide range of control signal, and small chip size characteristics. The VGA is fabricated in 0.18 $\mu\text{m}$  CMOS technology and measurements show a gain variation of 83dB (-36~47dB) with a gain error of less than  $\pm 2\text{dB}$ . The P1dB and IIP3 vary from -55 and -20 to 8 and 20.5dBm, respectively. The 3-dB bandwidth is from 37 to 420MHz. The current dissipation is less than 3.4mA from 1.8V supply voltage. The chip occupies 0.4mm<sup>2</sup>.

**Keywords:** Variable gain amplifier (VGA), automatic gain control (AGC), wireless transceiver

## I. INTRODUCTION

Variable gain amplifier (VGA) is an important block at the front end of many communication systems to maximize the dynamic range of the receivers. In wireless communication systems, the amplitudes of the receiver and transmitter signals vary by a large amount such that a very wide gain control range VGAs are needed. For example, the CDMA receiver requires at least 80dB of the dynamic gain range.

The VGAs in wireless transceivers are usually embedded in an automatic gain control circuit (AGC) to provide an output signal with constant amplitude. Therefore, to minimize the settling time of AGCs, the gain of VGAs has to be an exponential function of the control signal. Unfortunately, it is difficult to generate an exponential transfer function in CMOS technology due to square-law characteristics of MOSFETs in the saturation-mode. The MOSFETs show the exponential characteristics in weak inversion but can be adopted only for very low-frequency applications. Therefore, many researches to achieve dB-linear gain variation characteristics of the VGA in CMOS technology have been reported; such as master-slave control and signal-summing techniques [1, 2], or using Taylor concept and pseudo-exponential generator for realizing the dB-linear gain characteristic [3-6]. However, the master-slave control technique obtains a gain variation range of less than 20dB per one-stage VGA [1]. The VGAs that adopt the Taylor concept and the pseudo-exponential generator even exhibits less amount of gain control range, which is 12 and 15dB with a gain error of less than  $\pm 0.5\text{dB}$ , respectively [3-6]. Owing to the limitation of the gain range of the CMOS-based

VGAs in recent researches, the multiple-stage VGAs are used to satisfy the requirement of the gain variation of communication systems (for example, to offer 80dB gain control range: 4 gain stages for master-slave control technique, 6 gain stages for pseudo-exponential generator VGA, and 7 gain stages for Taylor concept approach). Obviously, the multi-stage VGAs result in high power consumption and a large chip size (or high cost).

Since the  $I$ - $V$  characteristic of bipolar transistors follows an exponential function. The VGA, adopting bipolar transistors, is expected to provide a wide control gain range [2]; but the bipolar techniques are not compatible with standard CMOS-based circuits [2], while BiCMOS is not a cost-efficient solution.

The idea of implementing bipolar transistors in conventional CMOS technology have been studied and adopted for circuits like bandgap voltage reference and emitter followers to drive capacitive line on SRAM chips [7, 8, 9]. In this paper, the bipolar transistor, created in CMOS technology, generates the exponential current to control the gain of the VGA. The newly proposed VGA topology uses a PMOS transistor with the body terminal as a control signal for varying the gain, which results in a wide gain control range, a wide variation of the control signal, and low-power consumption. Moreover, the proposed VGA utilized a linearization technique to improve the linearity.

## II. REALIZATION OF BIPOLAR TRANSISTOR IN CONVENTIONAL CMOS TECHNOLOGY

As in [7], the parasitic bipolar transistors can be realized in conventional CMOS technology without any modification of the IC process as shown in Fig. 1. Two collectors are available on such a bipolar: the vertical to substrate which is always exists in the well, and the lateral, which is constituted by the source and drain terminals of the conventional PMOS transistor. These two bipolars share the base terminal, which is also the body terminal of PMOS transistor. The current flowing from terminal E to C1 and C2 in Fig. 1 is an exponential function of the voltage between E and B terminals, and can be given by

$$I_{EC} = I_s e^{\left(\frac{V_{BE}}{\eta kT/q}\right)} \quad (1)$$

This current will be used to control the gain of the VGA as discussed later in this paper.

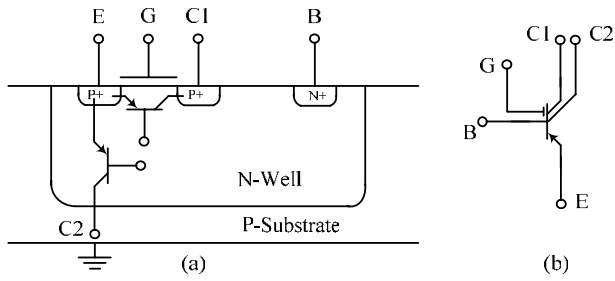


Fig. 1 Realization of bipolar in conventional PMOS transistor

### III. NEWLY PROPOSED HIGH LINEARITY VGA TOPOLOGY

The proposed circuit of the low-power and high linearity VGA is shown in Fig. 2, which is composed of a variation gain and a common-mode feedback circuits. The variable gain circuit is composed of an input source-coupled pair ( $M_1$  and  $M_2$ ) and diode-connected loads ( $M_3$  and  $M_4$ ). The gain of the amplifier in Fig. 2 can be expressed as

$$A_v = \frac{g_{m-input}}{g_{m-load}} = \frac{\sqrt{(W/L)_{input} I_{bias}}}{\sqrt{(W/L)_{load} I_{ctrl}}} \quad (2)$$

where  $g_{m-input}$  is the transconductance of the input transistors ( $M_1$  and  $M_2$ ),  $g_{m-load}$  the transconductance of the diode

connected loads ( $M_3$  and  $M_4$ ). The transistor  $M_8$  in Fig. 2 is characterized by two bipolar transistors as shown in Fig. 1. The terminals E, C, and B in Fig. 1 are respectively corresponding to the source, drain, and body terminals of the transistor  $M_8$  as shown in Fig. 2. Therefore, the  $I_{ctrl}$  in Fig. 2 is the same as the  $I_{EC}$ , which is given in (1).

Assume that  $(W/L)_{input} = (W/L)_{load}$ , from (1) and (2) the gain of the proposed VGA is calculated as

$$A_v = \frac{g_{m-input}}{g_{m-load}} = \sqrt{I_{bias}} \times I_s e^{\frac{1}{2} \left( \frac{V_{ctrl} - V_E}{\eta kT/q} \right)} \quad (3).$$

From (3), the differential gain of the proposed VGA is an exponential function of the control signal  $V_{ctrl}$ . The bias current  $I_{bias}$  does not affect the gain variation range. The gain of the proposed VGA given in (3) is obvious not a function of process parameters. In other words, the gain of the proposed VGA is independent on process variations.

In Fig. 2, the currents, flowing through the upper PMOS current sources ( $M_5$  and  $M_6$ ), are equal to the sum of the currents of the input source-coupled and diode-connected pairs. From Fig. 2, the sum of the currents through  $M_5$  and  $M_6$  is  $(I_{bias} + I_{ctrl})$ , which is an exponential function of the control signal, resulting in the unstable output common-mode voltage. Consequently, the common-mode feedback circuit with a high gain is needed to stabilize the output common mode level as shown in Fig. 2.

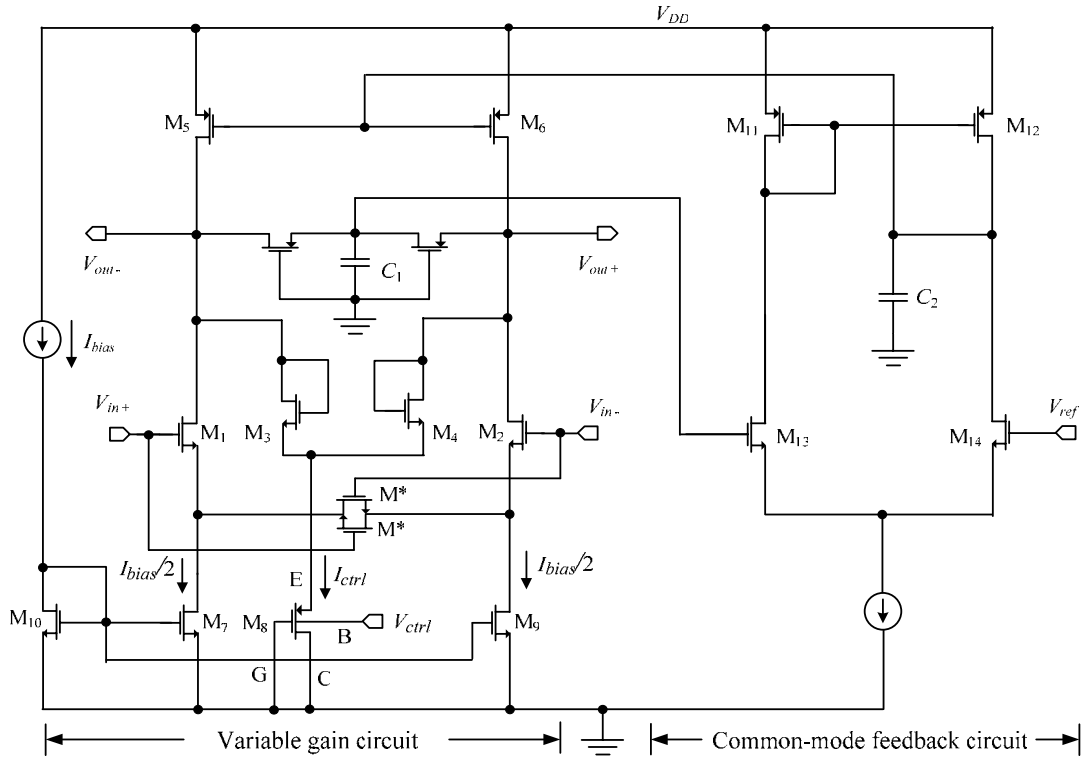


Fig. 2 The complete schematic of the newly proposed VGA

In order to avoid interference with adjacent channels in wireless communication systems, the VGA is imposed by high linearity characteristic. One of the useful techniques to improve the linearity of the differential amplifier is using MOS transistors as source degeneration [10]. In the proposed VGA, the transistor  $M^*$  in Fig. 2 functions as source degeneration transistors which help to improve the linearity. The proposed VGA is compact, leading to low-power consumption.

Fig. 3 shows the block diagram of the overall VGA. The VGA adopts three amplifying blocks in cascade. In Fig. 3, all VGA cells use the same circuit shown in Fig. 2. The buffer in Fig. 3 is added for the conveniences of the measurements, providing high input and  $50\Omega$  output impedances.

Regarding the frequency response, assuming that the VGA would be evaluated under  $50\Omega$  environment, the bandwidth of the VGA is dominated by the pole at the inter-stage node between two amplifiers. Since the resistance from the inter-stage node to the AC ground is dominated by the diode-connected transistors  $M_3$  and  $M_4$ , this resistance varies as a function of the gain, the bandwidth of the amplifier varies correspondingly. At higher gains the current flowing through the diode-connected transistor is reduced leading to narrower bandwidths.

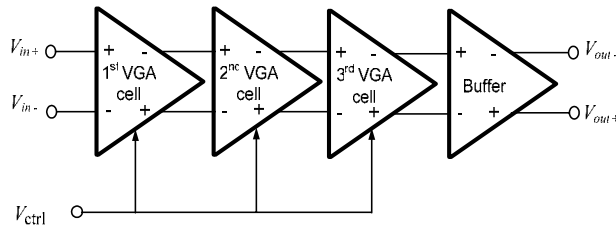


Fig. 3 Block diagram of the proposed 3-stage VGA.

#### IV. MEASUREMENT RESULTS

In  $0.18\mu\text{m}$  CMOS technology, the three-stage VGA dissipates an average current of less than  $3.4\text{mA}$  from  $1.8\text{V}$  supply voltage. The measured control current  $I_{ctrl}$  versus  $V_{ctrl}$  is depicted in Fig. 4. As shown in Fig. 4, the  $I_{ctrl}$  is an exponential function of  $V_{ctrl}$ . Fig. 5 shows the measured gain as a function of  $V_{ctrl}$ , the gain of the proposed VGA varies from  $-36$  to  $47\text{dB}$  over a wide range of  $V_{ctrl}$ , which is from  $0$  to  $1.8\text{V}$ . Fig. 6 shows the frequency response of the proposed VGA for different  $V_{ctrl}$ . In Fig. 6, the  $3\text{-dB}$  bandwidth is  $37\text{MHz}$  at the maximum gain of  $47\text{dB}$ , and is widening as the gain is reduced. The maximum  $3\text{-dB}$  bandwidth is  $420\text{MHz}$  at the minimum gain of  $-36\text{dB}$ .

The measured  $\text{P1dB}$  and  $\text{IIP3}$  versus the gain of the proposed VGA are shown in Fig. 7, by implementing the linearization technique, the VGA obtain good linearity characteristics. As depicted in Fig. 7 the maximum and minimum  $\text{P1dB}$  are measured respectively as  $-55$  and  $8\text{dBm}$ , and the  $\text{IIP3}$  varies from  $-20$  to  $20.5\text{dBm}$ . The overall VGA

performance is summarized in Table. I. The layout of the proposed VGA is depicted in Fig. 8, which is  $0.4\text{mm}^2$ .

#### V. CONCLUSIONS

The VGA topology is newly proposed, implemented, and verified through the measurement. The PMOS transistor with the body terminal as the control signal for varying the gain is utilized. With the proposed idea, a very wide gain variation is obtained so that fewer VGA stages are needed to satisfy the required  $\text{dB}$  gain range of communication systems. Consequently, the chip size (or the cost) and the power consumption are reduced. The proposed VGA shows a good linearity characteristic. In  $0.18\mu\text{m}$  CMOS technology, the VGA exhibits good performances at low-power applications as summarized in table. I. The three-stage VGA can offer a very wide control gain range ( $83\text{dB}$ ) over a wide range of the control signal  $V_{ctrl}$  ( $0 \sim 1.8\text{V}$ ). The gain is independent on process variation. The current dissipation is  $3.4\text{mA}$  and the chip size is  $0.4\text{mm}^2$ . The  $3\text{-dB}$  bandwidth is from  $37$  to  $420\text{MHz}$ .

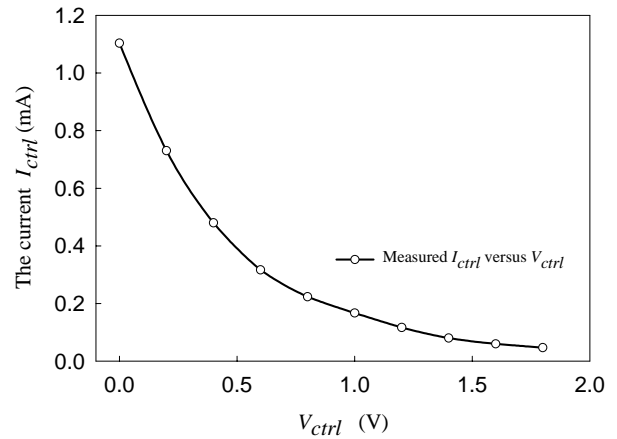


Fig. 4 The measured  $I_{ctrl}$  versus  $V_{ctrl}$

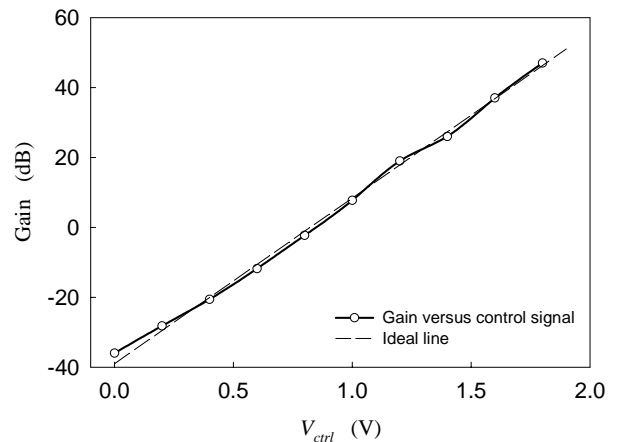


Fig. 5 Measured gain versus control voltage  $V_{ctrl}$

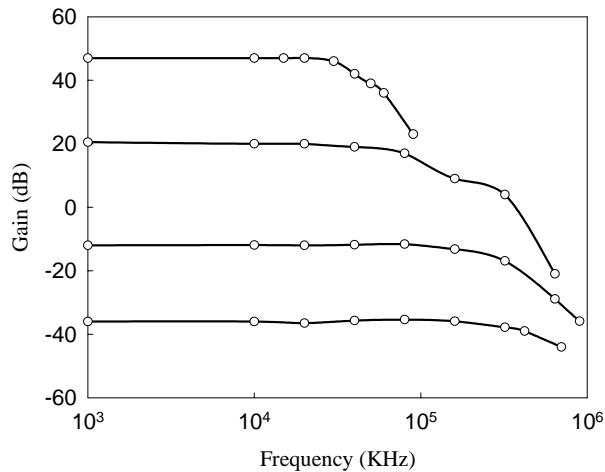


Fig. 6 Measured frequency response for different control signal voltage  $V_{ctrl}$

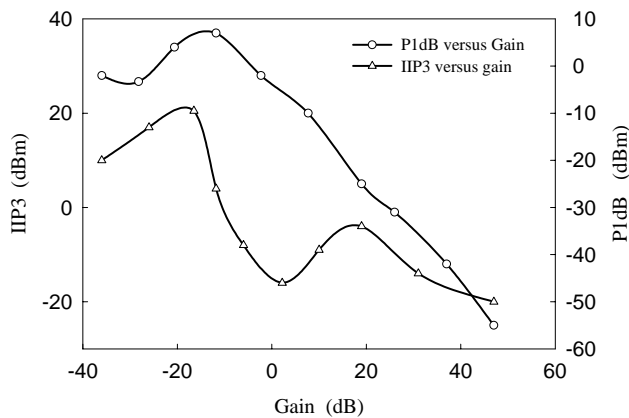


Fig. 7 Measured P1dB and IIP3 versus the gain of the proposed VGA

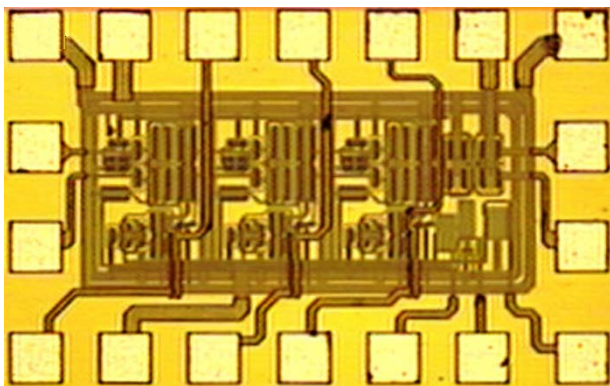


Fig. 8 The proposed three-stage VGA photo

TABLE I  
SUMMARY OF MEASUREMENT RESULTS

Technology	0.18 $\mu$ m
Chip area	0.4mm <sup>2</sup>
Power consumption excluding the buffer	3.4mA/1.8V
3dB-Bandwidth	37~420MHz
Gain range	-36 ~47dB
Gain error	$\pm$ 2dB
Input P1dB	-55~8dBm
IIP3	-20~20.5dBm
Input/output impedances	50 $\Omega$

#### ACKNOWLEDGEMENTS

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#### REFERENCES

- [1] T. Yamaji, N. Kanou and T. Itakura, "A Temperature-Stable CMOS Variable-Gain Amplifier with 80-dB Linearly Controlled Gain Range," *J. of Solid-State Circuits*, vol. 37, no. 5, pp553-558, May. 2002.
- [2] S. Otaka, G. Takemura, and H. Tanimoto, "A Low-Power Low-Noise Accurate Linear-in-dB Variable-Gain Amplifier with 500-MHz Bandwidth," *J. of Solid-State Circuits*, vol. 35, no. 12, pp1942-1948, Dec. 2000.
- [3] Christopher W. M, "A Variable Gain CMOS Amplifier with Exponential Gain Control," *Dig. Symp. VLSI Circuits*, pp. 146-149, 2000.
- [4] P. Huang, L.Y. Chiou, and C.K. Wang, "A 3.3-V CMOS Wideband Exponential Control Variable-Gain-Amplifier," *Inter. Sym. On Cir. and Syst.*, pp. I-285-I-288, May 1998.
- [5] M. M. Green and S. Joshi, "A 1.5-V CMOS VGA Based on Pseudo-Differential Structures," *Inter. Sym. On Cir. and Syst.*, pp. IV-461-IV-464, May 2000.
- [6] C.-C Chang, M.-L. Lin, and S.-I. Liu, "CMOS Current-mode Exponential-Control Variable-Gain Amplifier," *IEE Electronics Letters*, vol. 37, no. 14, pp 868-869, July 2001.
- [7] T. W. Pan and A. A. Abidi, Member, IEEE, "A 50-dB Variable Gain Amplifier Using Parasitic Bipolar Transistor in CMOS," *J. of Solid-State Circuits*, vol. 24, No. 4, pp951-961, Aug. 1989.
- [8] Y. P. Tsvividis and R. W. Ulmer, "A CMOS voltage reference," *IEEE J. of Solid-State Circuits*, vol. SC-20, pp774-778, Dec. 1978.
- [9] O. Minato et al., "A high speed low power Hi-CMOS 4K static RAM," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 882-885, June 1979.
- [10] F. Krummenacher and N. Joehl, "A 4-MHz CMOS Continuous-time Filter with On-Chip Automatic Tuning", *J. of Solid-State Circuits*, vol. 23, No. 3, pp750-758, June. 1988.